## REMARKS/ARGUMENTS

Reconsideration and re-examination are hereby requested.

Claims 51, 53, 55, 57 and 59 have been amended to remove the term "server" since such term had not been used in the patent application. It should be understood however that the invention applies to systems having a server.

It is noted that in accordance with one feature of the present invention there is "end user data" and "interface state data". End user data is data that passes either from the host computer to the bank of disk drives or from the bank of disk drives to the host computer. Interface state data is data that controls the internal operation of the interface between the host computer and the bank of disk drives.

In accordance with one feature of the invention, see claim 52, ***end user data*** passes ***to and from the cache memory*** through ***an end user data communication channel*** in response ***to interface state data passing through the directors*** through ***a different, interface state data communication channel***. With the system shown in FIG. 1 of the patent application, the end-user data and interface state data are transferred among the directors and the cache memory on busses. The transfer of each word, whether a burst of end-user data or an interface state data passes through the interface in the same manner; i.e., requiring a fixed amount of overhead, i.e., bus arbitration, etc.

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG., 1 of the patent application so that ***end user data*** (i.e., data which passes either from the host computer to the bank of disk drives or from the bank of disk drives to the host computer) and ***interface state data*** (i.e., data that controls the internal operation of the interface between the host computer and the bank of disk drives) ***pass through different communication channels*** as set forth in claim 52.

More particularly, and referring to the Background section of the patent application, beginning at page 2, line 29, in operation, when the host computer wishes to store end-user (i.e., host computer) data at an address, the host computer issues a write request to one of the front-end directors to perform a write command. One of the front-end directors replies to the request and asks the host computer for the data. After the request has passed to the requesting one of the front-end directors, the director determines the size of the end-user data

and reserves space in the cache memory to store the request. The front-end director then produces control signals on either one of the busses connected to such front-end director. The host computer then transfers the data to the front-end director. The front-end director then advises the host computer that the transfer is complete. The front-end director looks up in a Table, not shown, stored in the cache memory to determine which one of the rear-end directors is to handle this request. The Table maps the host computer address into an address in the bank of disk drives. The front-end director then puts a notification in a "mail box" (not shown and stored in the cache memory) for the rear-end director which is to handle the request, the amount of the data and the disk address for the data. Other rear-end directors poll the cache memory when they are idle to check their "mail boxes". If the polled "mail box" indicates a transfer is to be made, the rear-end director processes the request, addresses the disk drive in the bank, reads the data from the cache memory and writes it into the addresses of a disk drive in the bank. When end-user data previously stored in the bank of disk drives is to be read from the disk drive and returned to the host computer, the interface system operates in a reciprocal manner. The internal operation of the interface, (e.g. "mail-box polling", event flags, data structures, device tables, queues, etc.) is controlled by interface state data which passes between the directors through the cache memory. Further, end-user data is transferred through the interface as a series of multi-word transfers, or bursts. Each word transfer in a multi-word transfer is here, for example, 64 bits. Here, an end-user data transfer is made up of, for example, 32 bursts. Each interface state word is a single word having, for example, 64 bits.

It is first noted that the end-user data and interface state data are transferred among the directors and the cache memory on the busses. The transfer of each word, whether a burst of end-user data or an interface state data passes through the interface in the same manner; i.e., requiring a fixed amount of overhead, i.e., bus arbitration, etc. Each one of the two busses must share its bandwidth with both end-user data and the interface state data. Therefore, the bandwidth of the system may not be totally allocated to end-user data transfer between the host computer and the bank of disk drives.

***In accordance with the feature of the invention*** described above, ***end user data*** passes ***to and from the cache memory*** through ***an end user data communication channel*** in response ***to interface state data passing through the directors*** through ***a different, interface***

***state data communication channel***.

With such an arrangement, the system bandwidth is increased ***because end-user data and interface state data are carried on separate bus systems within the interface.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application so that ***end user data*** (i.e., data which passes either from the host computer to the bank of disk drives or from the bank of disk drives to the host computer) and ***interface state data*** (i.e., data that controls the internal operation of the interface between the host computer and the bank of disk drives) ***pass through different communication channels*** as set forth in claim 52.

Referring now to the other independent claims:

Claim 11 points out that the system includes: an interface state data bus section, for carrying interface state data, such interface state data bus section being in communication with both: a) the at least one front-end one and the at least one rear-end one of the directors; and (b) the memory; a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the memory; and

***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors via the interface state data bus section.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide an arrangement ***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors via the interface state data bus section.***

Claim 20 points out that the method includes: providing a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second

end coupled to the memory; and ***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors via the interface state data bus.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide an arrangement ***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors via the interface state data bus section.***

Claim 21 points out that the system includes and arrangement ***wherein the central processing units of the plurality of directors control the end-user data transfer between the host computer and the bank of disk drives via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors via the interface state data bus section.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide an arrangement wherein the central processing units of the plurality of directors control the end-user data transfer between the host computer and the bank of disk drives via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors via the interface state data bus section.

Claim 29 points out that the method includes providing an interface state data section for carrying interface state data, such interface state data section being in communication with the at least one front-end one and the at least one rear-end one of the directors; providing a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the memory; and ***wherein such central processing units of the plurality of directors control the end-user data transfer between the***

***host computer and the bank of disk drives and the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 30 points out that the system includes an interface state data bus section, for carrying interface state data, such interface state data bus section being in communication with both the front-end portion of the plurality of directors and the rear end portion of the plurality of directors; a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the memory; and ***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 39 points out that the method includes providing an interface state data section for carrying interface state data, such interface state data section being in communication with the front end portion of the directors and the rear end portion of the directors; providing a plurality of end-user data busses, for carrying end-user data, each one of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of directors and a second end coupled to the memory; and ***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives and the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 40 points out that the system includes: an interface state data bus section, for carrying interface state data, such interface state data bus section being in communication with both the front-end portion of the plurality of directors and the rear end portion of the plurality of directors; a plurality of end-user data busses, for carrying end-user data, each one of a first portion of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of front end directors and a second end coupled to the memory and each one of a second portion of the plurality of end user data buses having a first end coupled to a corresponding one of the plurality of rear end directors and a second end coupled to the memory; and ***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives through the memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 44 points out that the method includes: providing an interface state data section for carrying interface state data, such interface state data section being in communication with the plurality of front end directors and the plurality of rear end directors; providing a plurality of end-user data busses, for carrying end-user data, each one of a first portion of the plurality of end-user data busses having a first end coupled to a corresponding one of the plurality of front end directors and a second end coupled to the memory and each one of a second portion of the plurality of end user buses having a first end coupled to a corresponding one of the plurality of the rear end directors and a second end coupled to the memory; ***wherein the central processing units of such plurality of directors control the end-user data transfer between the host computer and the bank of disk drives and the***

***memory via the end-user data busses in response to interface state data generated by the directors, such generated interface state data being transferred among the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 48 points out that the system includes: a plurality of directors, each one of the directors having an end user data port and an interface state data port; a cache memory coupled to the end user data ports of the plurality of directors; ***wherein the directors control end user data transfer with end user data in such end user data transfer passing through the cache memory in response to interface state data passing through the interface state data ports of the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 49 points out that the system includes: a cache memory coupled to the end user data ports of the plurality of first directors and second directors***; wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the cache memory in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 50 points out the system includes: a plurality of directors, each one of the directors having a n end user data port and an interface state data port; a cache memory; ***wherein the directors control end user data transfer with end user data in such end user data transfer passing to the cache memory through the end user data ports in response to interface state data passing through the interface state data ports of the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511

describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 51 points out that the system ***the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the end user data ports in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 52 points out, as noted above, ***that the directors control end user data transfer with end user data in such data transfer passing to the cache memory through an end user data communication channel in response to interface state data passing through the directors through a different, interface state data communication channel.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 53 points out that the system includes an arrangement wherein ***the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through an end user communication channel in response to interface state data passing between the first director and the second director through a different, interface state data communication path.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 54 points out that the system includes an arrangement wherein ***the directors control end user data transfer with end user data in such end user data transfer passing through the cache memory in response to interface state data passing through the interface state data ports of the directors.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an

arrangement.

Claim 55 points out that the system includes an arrangement wherein first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the cache memory in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 56 points out that the system includes an arrangement wherein directors control end user data transfer with end user data in such end user data transfer passing to the cache memory through the end user data ports in response to interface state data passing through the interface state data ports of the directors.

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 57 points out that the system includes an arrangement wherein the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through the end user data ports in response to interface state data passing between the first director and the second director through the interface state data ports of the plurality of first directors and the plurality of second directors.

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 58 points out that the system includes an arrangement ***wherein the directors control end user data transfer with end user data in such data transfer passing to the cache memory through an end user data communication channel in response to interface state data passing through the directors through a different, interface state data communication channel, one of such channels being coupled to a crossbar switch.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511

describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

Claim 59 points out that the system includes an arrangement wherein ***the first and second directors control end user data transfer between the host computer and the bank of disk drives with end user data in such end user data transfer passing through an end user communication channel in response to interface state data passing between the first director and the second director through a different, interface state data communication channel one of such channels being coupled to a crossbar switch.***

It is respectfully submitted that nothing in Murata et al., U. S. Patent No. 5, 386, 511 describes or suggests modifying FIG. 1 of the patent application to provide such an arrangement.

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Respectfully submitted,

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